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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,781	11/26/2003	Russell Alvin Schultz	SIG000103	9074

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EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,781	SCHULTZ ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to Amendment filed on 02/17/2006. Claims 1-19 are pending in this application. All rejections and objections not explicitly repeated below are withdrawn.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The rejections of claims 1-19 under 35 U.S.C. 102 (b) as being anticipated by Everett et al., US 6,220,510 B1 are maintained as shown below.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Everett et al., US 6,220,510 B1.

Regarding claim 1, Everett teaches that a method comprising:

allocating a first portion (Fig.1, static data space 103) of a first memory (it is taught as an application abstract machine AAM) as a static section to store a main program (col.5, lines 50-53) which uses functional programs (it is taught as each application for every transaction such as the card user's name, account number, PIN value and address) stored in a second memory (it is taught as IC card, col.3, lines 32-38); and

allocating a second portion of the first memory as a dynamic section (Fig.1, second portion is taught as volatile such as RAM) to store other programs (it is taught as temporary data which is used much like conventional computer programs, col.6, lines 8-16), the dynamic section including a plurality of overlay spaces (it is taught as dynamic or public segments) to overlay the functional programs loaded from the second memory to conserve memory capacity of the first memory (col.6, lines 8-16 and col.12, lines 21-31).

Regarding claim 2, Everett teaches that the allocating of the overlay spaces is determined by similar functions performed by the functional programs that are to be loaded into the overlay spaces (col.6, lines 39-42).

Regarding claim 3, Everett teaches that in allocating the overlay spaces, individual overlay spaces have entry and exit points for functional programs loaded into respective overlay spaces (col.5, lines 39-41 and col.8, lines 29-31).

Regarding claim 4, Everett teaches that further comprising accessing a functional program from the main program by specifying a resource identifier to identify a particular functional program (col.10, lines 6-20) and an entry address to identify an entry point into one of the overlay spaces (col.5, lines 39-41 and col.8, lines 29-31).

Regarding claim 5, Everett teaches that the allocating of the first and second portions are allocated on the first memory resident on an integrated circuit (col.3, lines 64 to col.4, lines 6) and the functional programs to be loaded into the overlay spaces are resident on the second memory external to the integrated circuit (col.4, lines 17-20).

Regarding claim 6, Everett teaches that a method comprising:

executing a program statement of a main program to perform a particular functional operation by identifying a corresponding functional program using a resource identifier (col.10, lines 6-20) and by specifying an entry point into one of the overlay spaces (col.5, lines 34-48 and col.8, lines 29-31);

using the resource identifier to identify a corresponding functional program to perform the particular functional operation (col.10, lines 6-20);

loading the functional program into an overlay space specified by the specified entry point (col.6, lines 25-48 and col.8, lines 29-31); and

executing the functional program in the overlay space (col.6, lines 39-48).

Regarding claim 7, Everett teaches that the loading the functional program into the overlay space loads the functional program into a specified overlay space assigned to program functions having similar performing tasks (col.6, lines 39-42).

Regarding claim 8, Everett teaches that using the resource identifier is achieved by loading the resource identifier into a register and reading the register to call the functional program into the specified overlay space(col.6, lines 25-33).

Regarding claim 9, Everett teaches that executing the functional program also includes calling at least one other functional program, in which functional programs are nested for overlaying (Fig.7A, 7B and 7C, col.12, lines 32 to col.13, lines 5).

Regarding claim 10, Everett teaches that further comprising returning to the main program after executing the functional program in the overlay space (it is taught as returning to the first applications as shown and described in Fig.7A, 7B and 7C, col.12, lines 32 to col.13, lines 5).

Regarding claims 11 and 15, Everett teaches that an apparatus comprising:

a first memory(it is taught as an application abstract machine AAM) having a first portion (Fig.1, static data space 103) as a static section to store a main program (col.5, lines 50-53) which uses functional programs (it is taught as each application for every transaction such as the card user's name, account number, PIN value and address) and

a second portion (Fig.1, second portion is taught as volatile such as RAM) as a dynamic section to store other programs which reside in the first memory (it is taught as temporary data which is used much like conventional computer programs, col.6, lines 8-16) for a shorter duration than the main program (col.2, lines 46-48), the dynamic section including a plurality of overlay spaces (it is taught as dynamic or public segments) to overlay functional programs(col.6, lines 8-16 and col.12, lines 21-31); and

a second memory (it is taught as IC card, col.3, lines 32-38) operably coupled to store the functional programs (col.3, lines 21 to col.4,lines 20) and to load a functional program specified by a resource identifier in the main program (col.10, lines 6-20) to a corresponding overlay space specified by an entry point specified by the main program (col.6, lines 25-48 and col.8, lines 29-31).

Regarding claims 12 and 16, Everett teaches that the first memory is a random access memory resident in an integrated circuit (it is taught as RAM within AAM) and the second memory is an external memory to the integrated circuit (it is taught as IC flash card, col.4, lines 53-58).

Regarding claims 13 and 17, Everett teaches that the second memory is larger in capacity than the first memory (col.4, lines 7-17), but in which the functional programs are loaded into the overlay spaces to allow overlay in use of the functional programs (col.4, lines 17-20).

Regarding claims 14 and 18, Everett teaches that individual overlay spaces are assigned to load program functions having similar performing tasks (col.6, lines 39-42).

Regarding claim 19, Everett teaches that the integrated circuit includes a register to load resource identifiers, which are then read to load the functional programs (col.6, lines 25-33).

Response to Applicant's Arguments

6. Applicant's arguments filed 02/17/2006 have been fully considered but they are not persuasive.

7. Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. In the applicant's remark filed on 02/17/2006, the applicant discussed the reference Everett as shown in the applicant's remarks, however, the applicant does not discuss the reference applied against the claims. The applicant must discuss the reference applied against the claims, explaining how the claims avoid the references or distinguish from them, however, the arguments on page 7,8 of remarks "Everett does not teach or suggest allocating...; Everett does not teach loading the functional program..." have only generic statement without specifically addressing the points set forth in the examiner's rejection.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

10. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 7:30-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 5/12/06

Jasmine Song

Patent Examiner

May 11, 2006

Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER